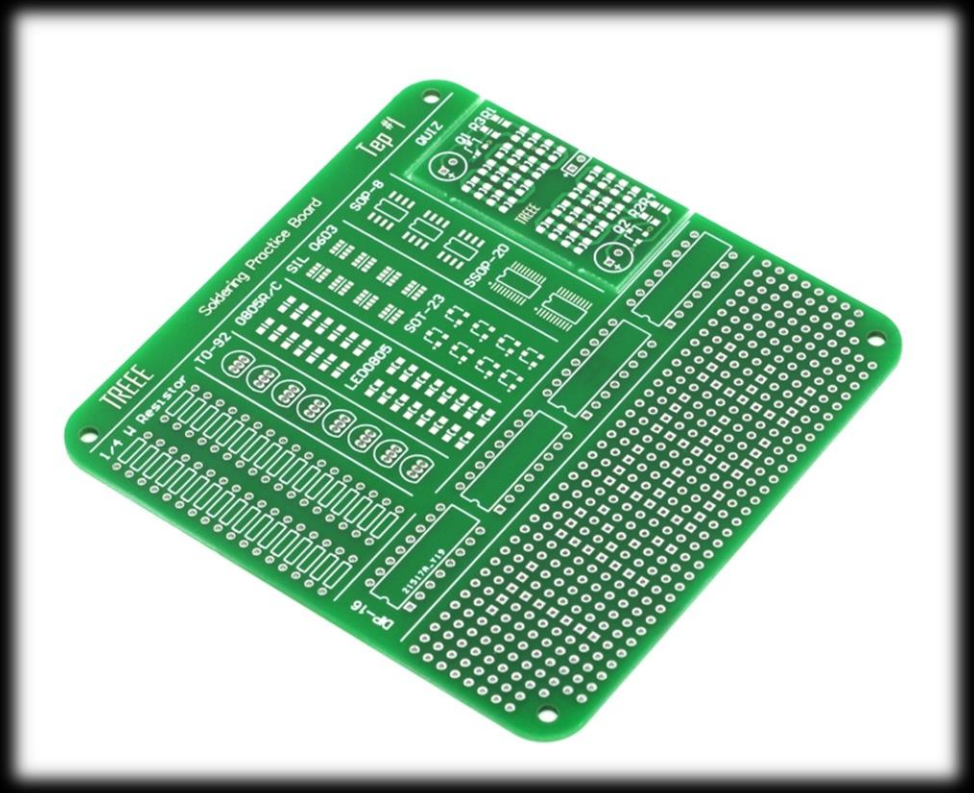
解决I/O数量不足的问题

程飞

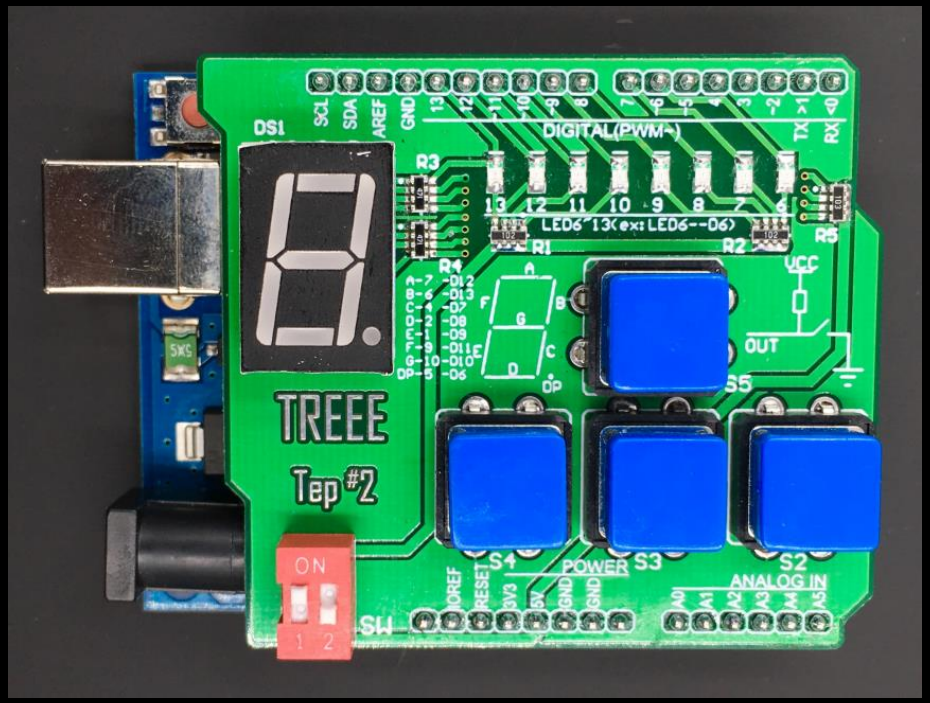
前情回顾 – TEP #1

- 历史与现实
- 焊接
  - 直插式元件
  - 贴片元件
  - 红蓝小警灯



前情回顾 - TEP #2

- 介绍了Arduino
- 串口通信
- 1位数码管的操作
- 独立按键操作

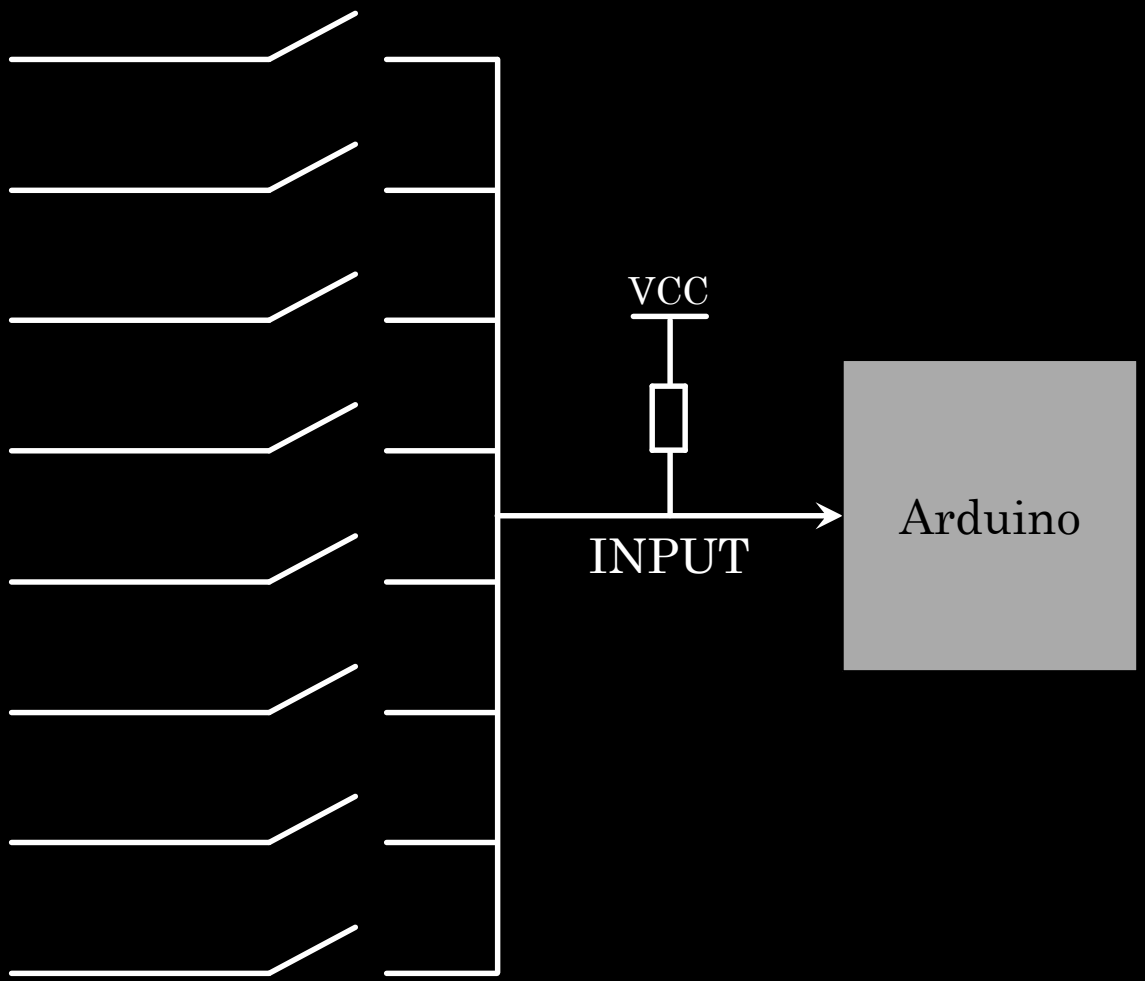


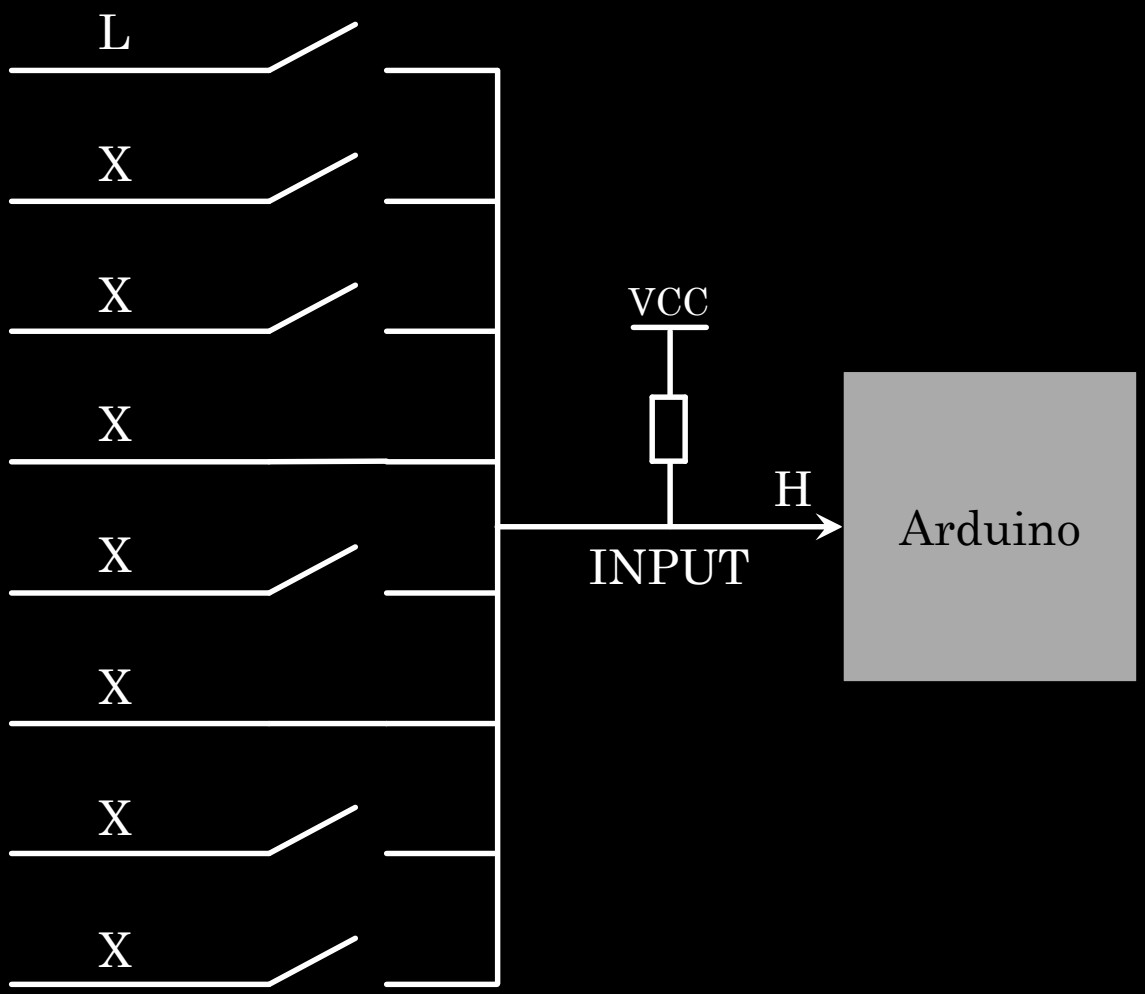
但是……

- 显示1位数字并没有什么大的作用
- 一个按键能实现的功能也非常有限
- 连一个计算器都做不出……
- 今天我们来控制16个按键和8位数码管

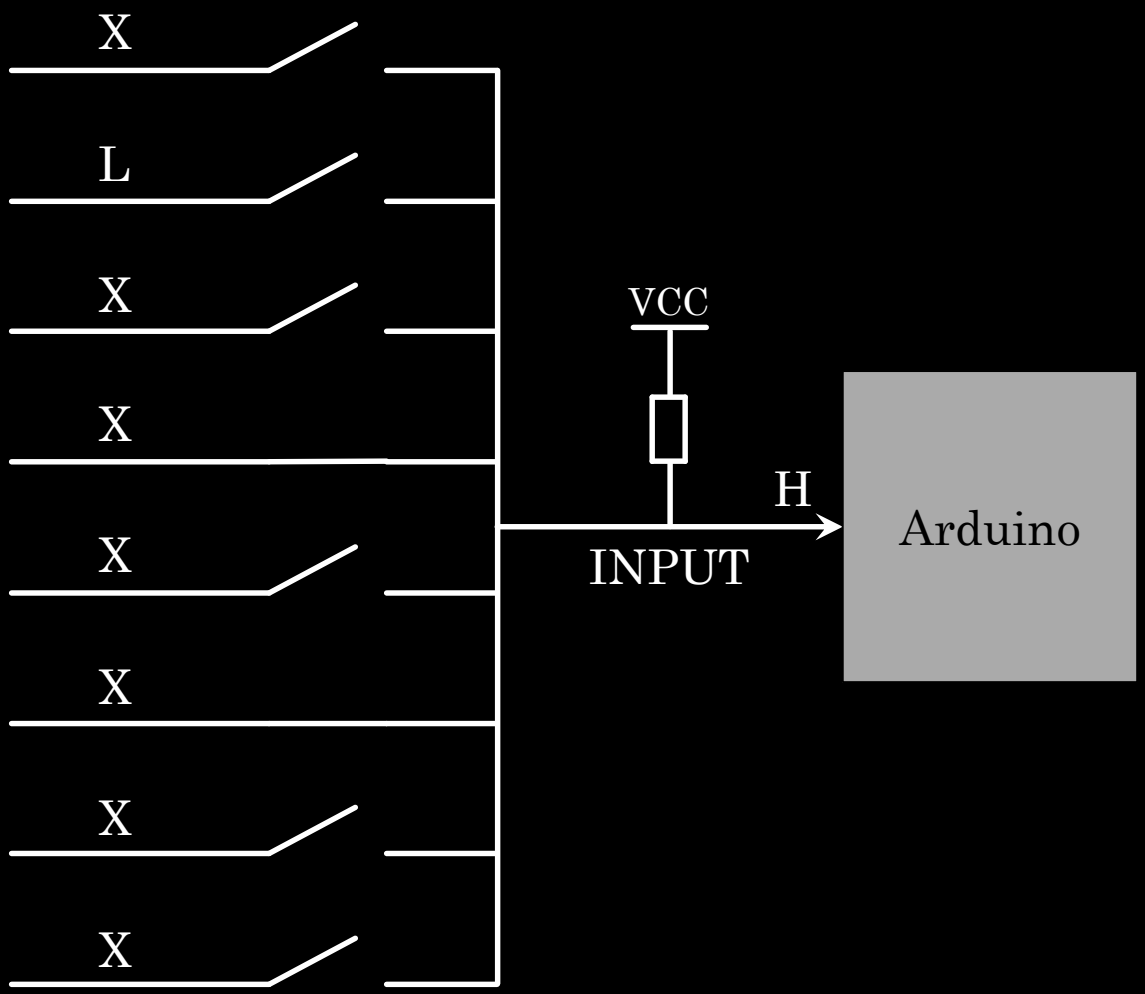
TEP #3 – 1 如何扩展单片机的I/O

- 思考一个简单的问题：
  - 假设目前单片机只有1个INPUT引脚，OUTPUT还有很多，现在我们要检测8个按键，应该怎么接线？


VCC
INPUT
Arduino



H：低电平
L：低电平
X：高阻态(断开)



H：低电平
L：低电平
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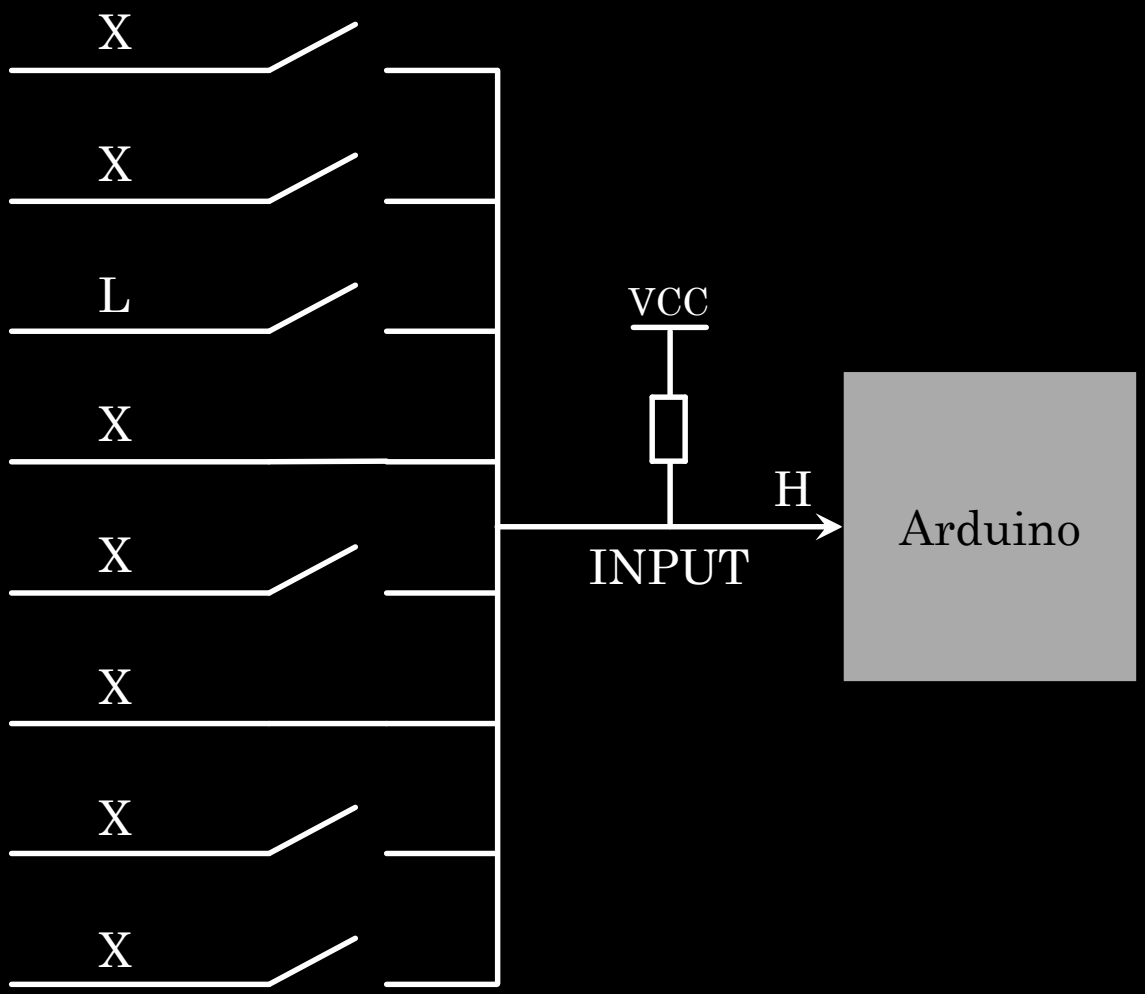

H：低电平
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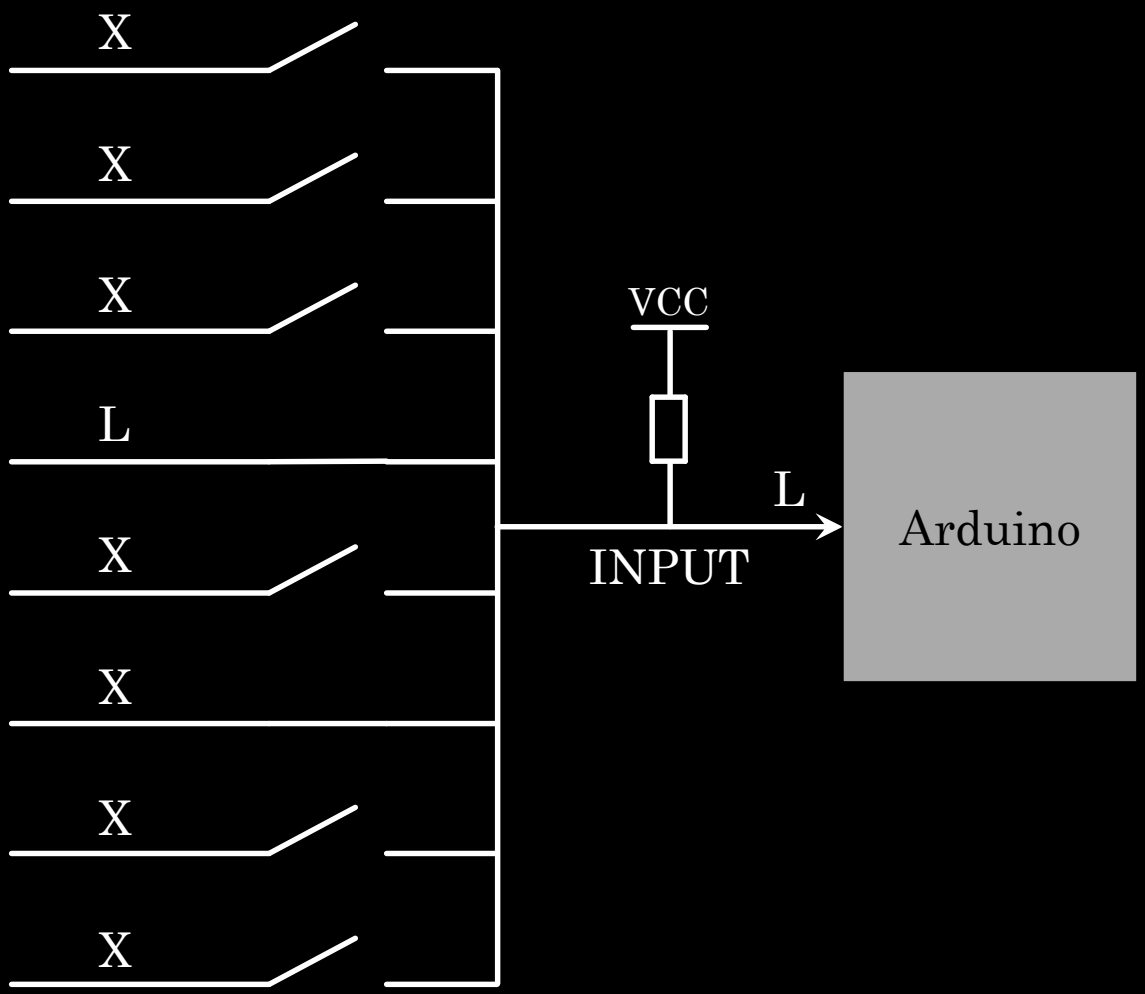

H：低电平
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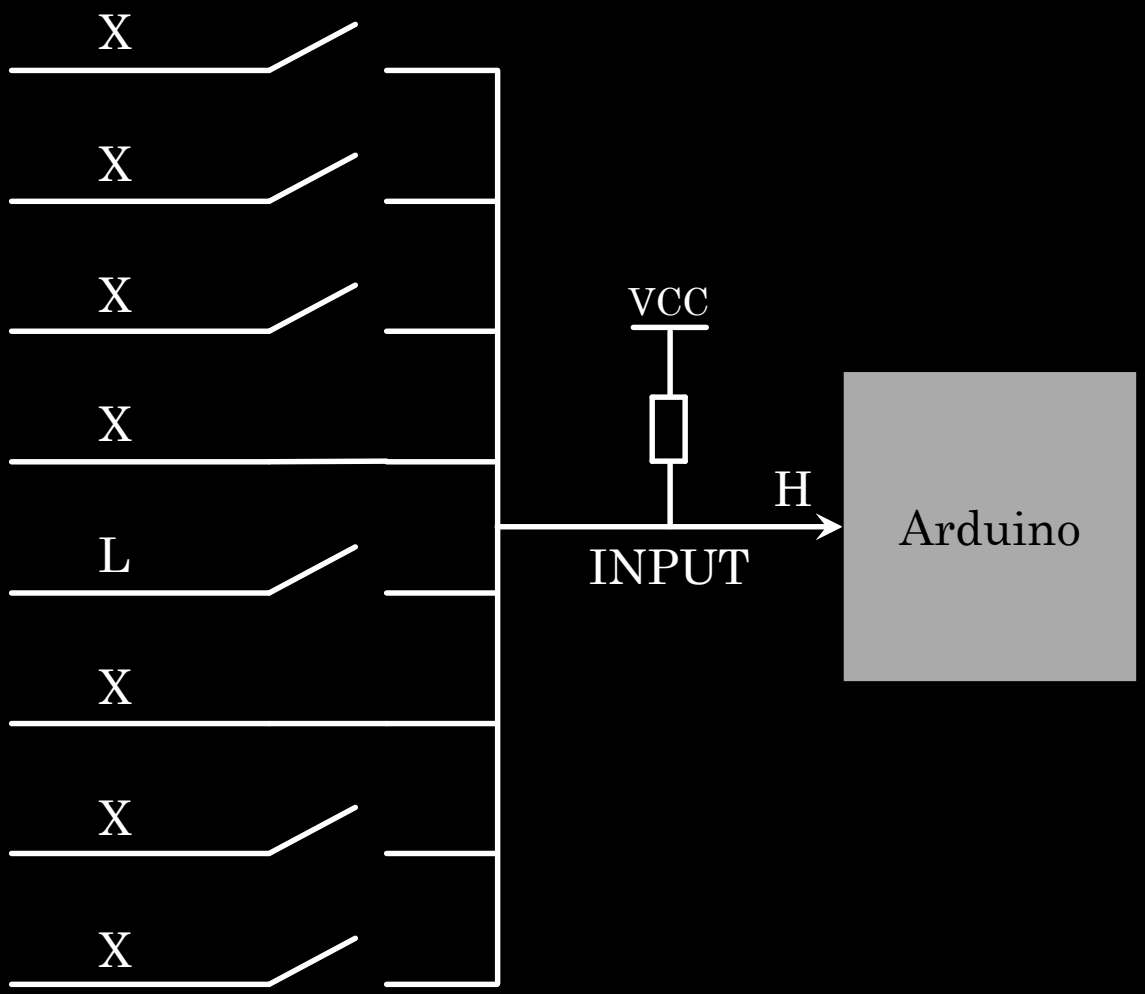
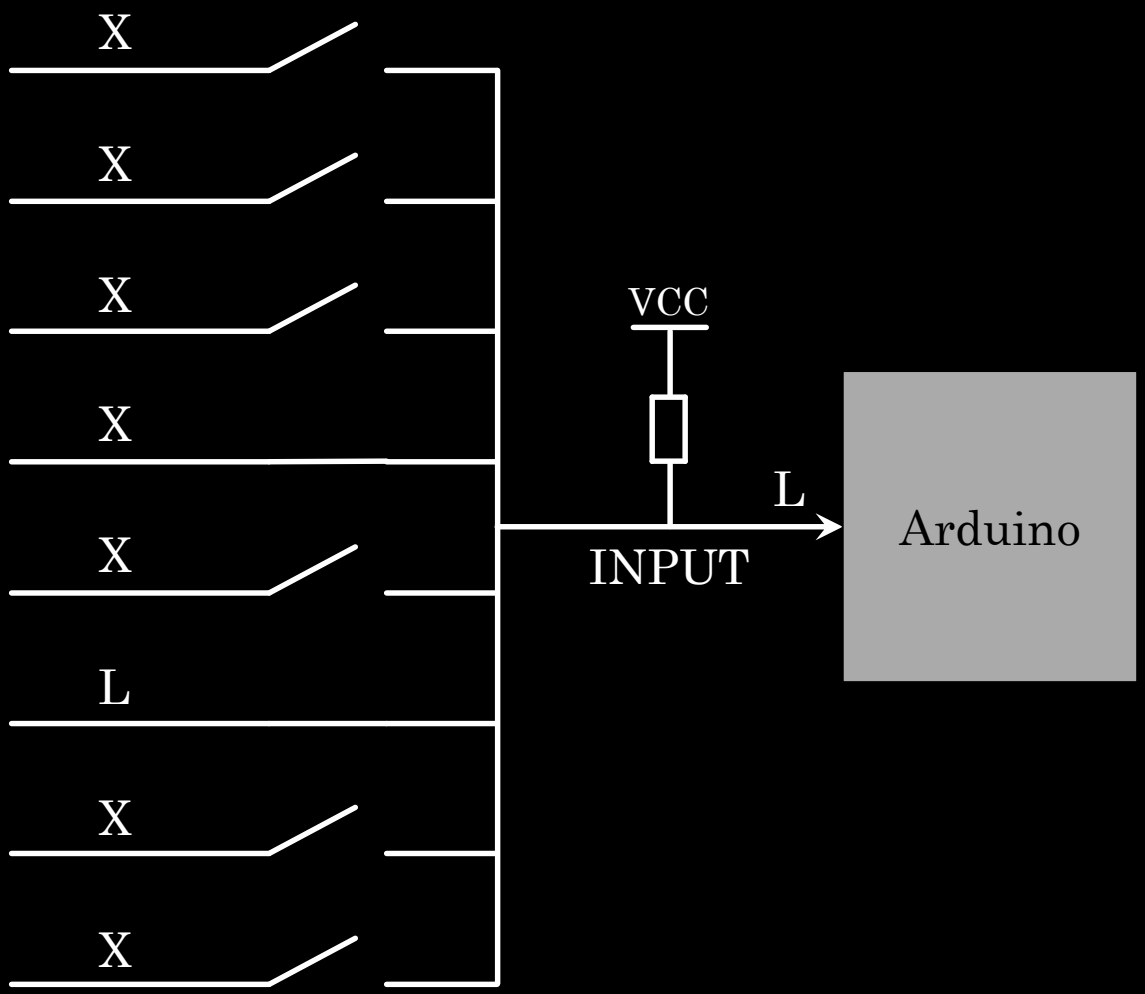
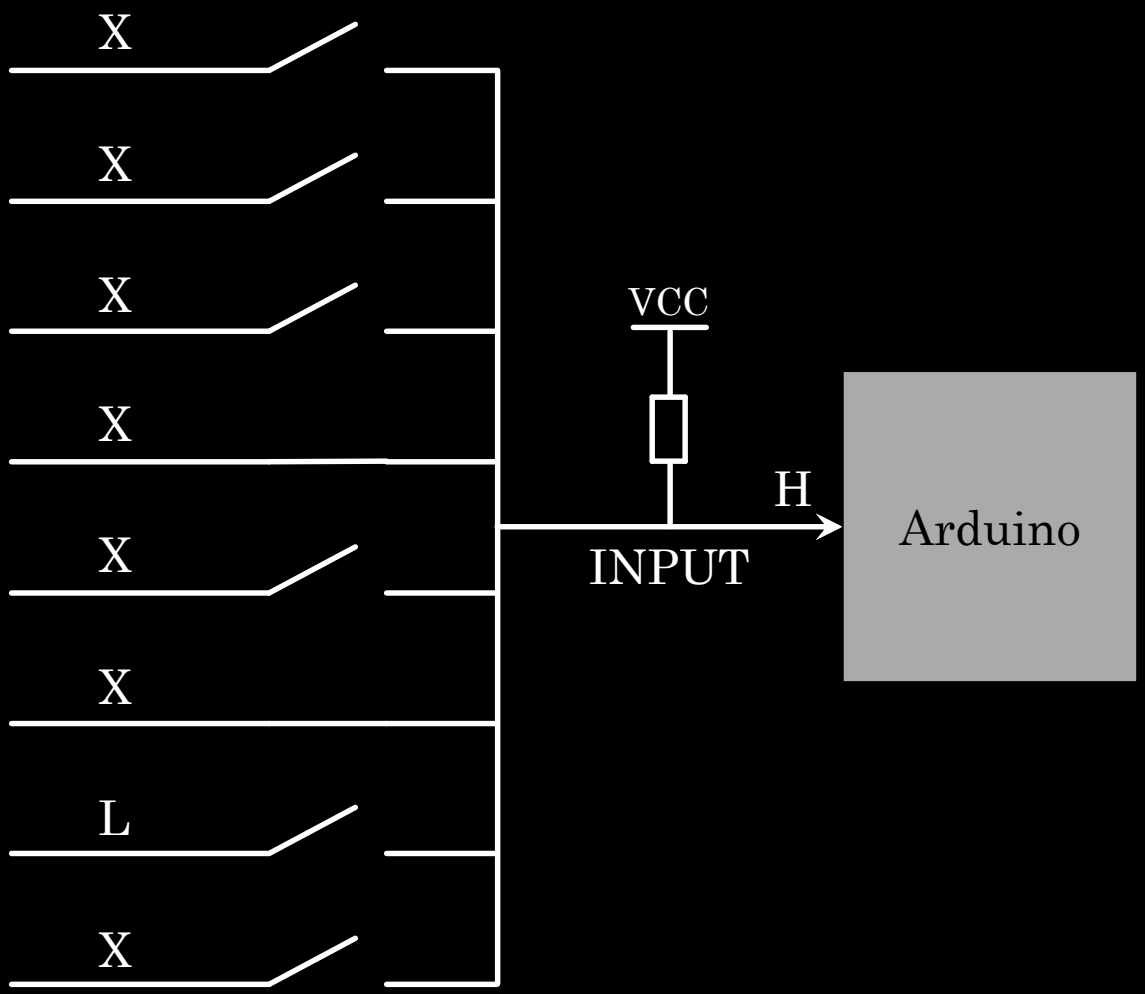
X：高阻态(断开)



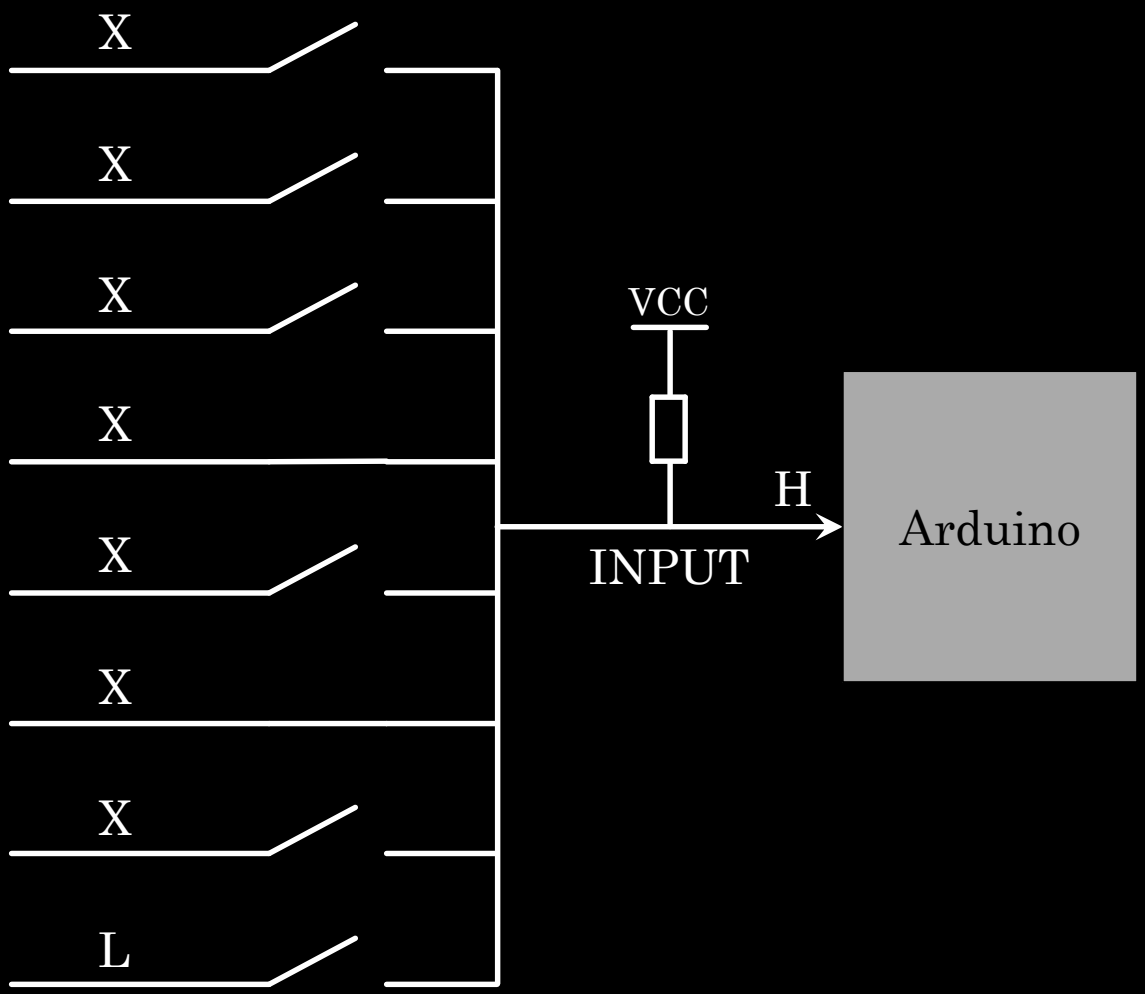
H：低电平
L：低电平
X：高阻态(断开)



H：低电平
L：低电平
X：高阻态(断开)



H：低电平
L：低电平
X：高阻态(断开)

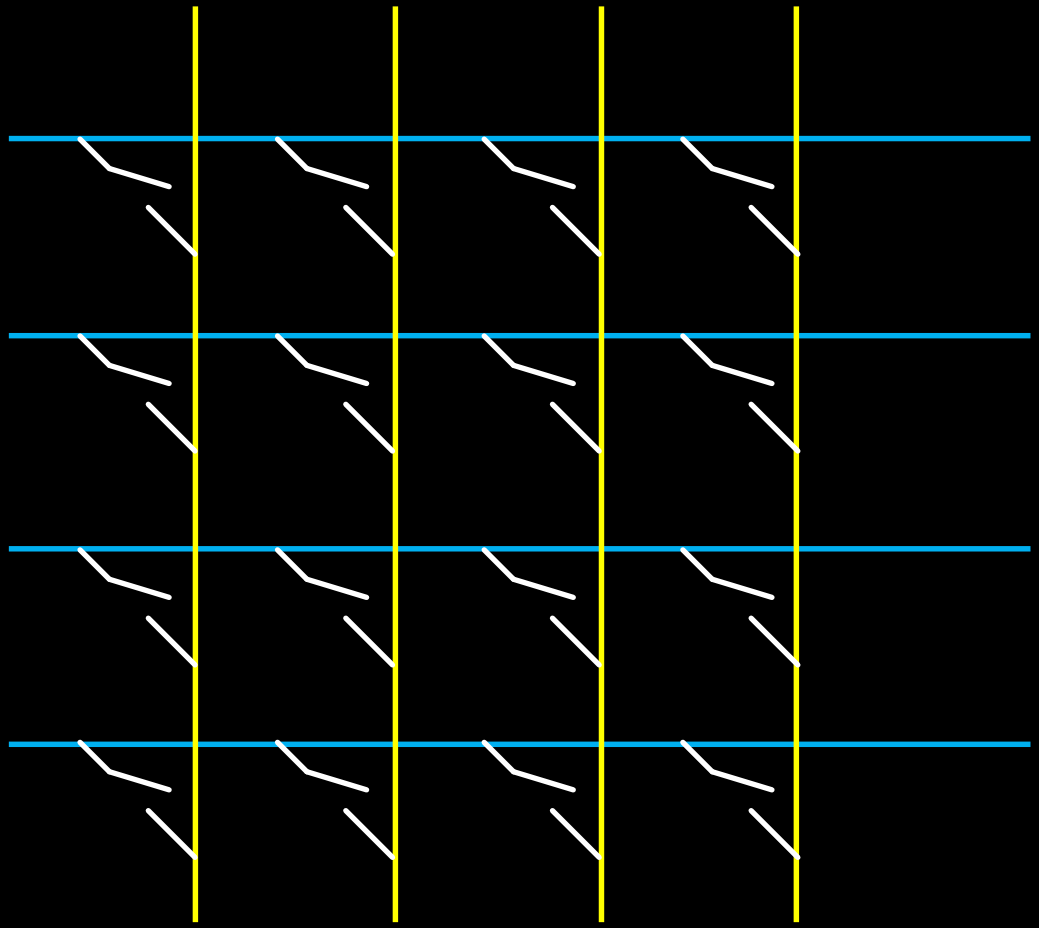


H：低电平
L：低电平
X：高阻态(断开)

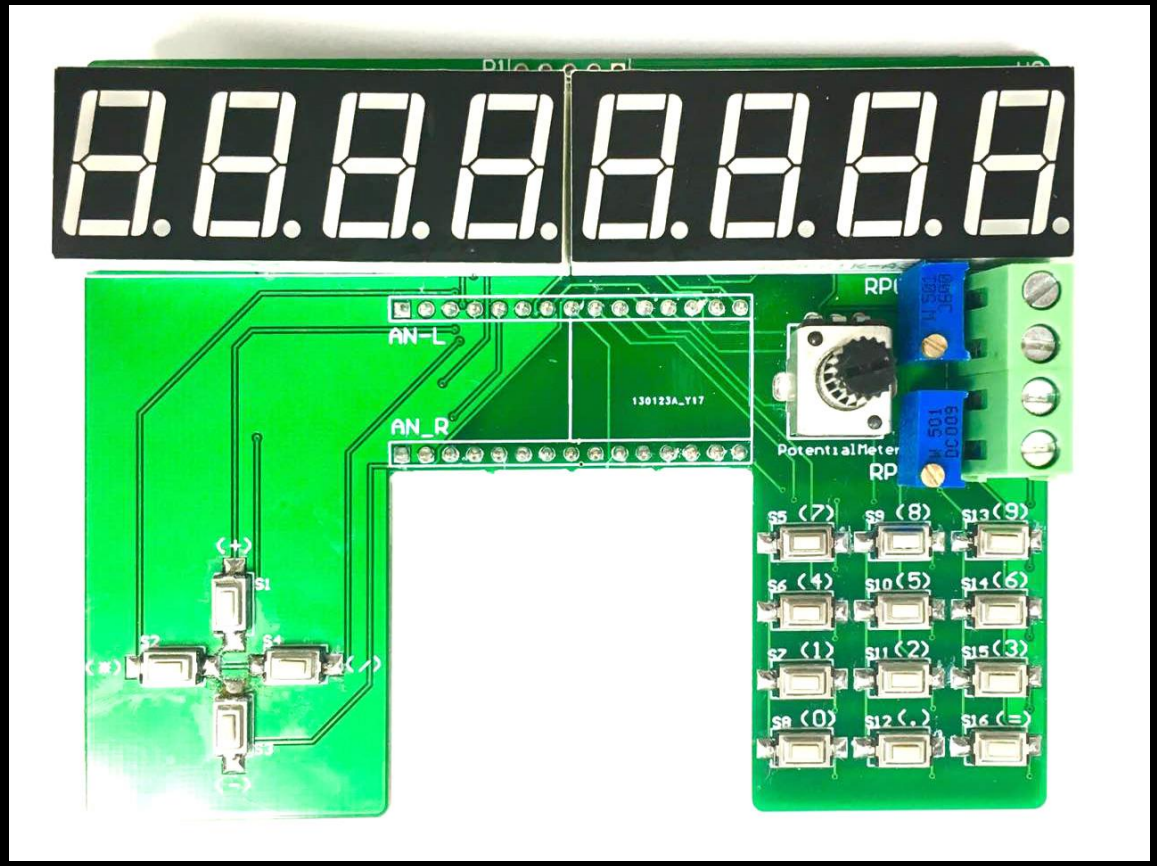
小结论

- 通过这种扫描的办法，可以用OUTPUT来节省INPUT的数量
- 不过看起来有点傻，一般的GPIO都同时可以INPUT和OUTPUT，按照这种办法需要用9个PIN，而原来的老办法也只需要8个PIN
- IN　OUT　按键　总共PIN
- 1　8　8　9
- 2　8　16　10
- 4　4　16　8

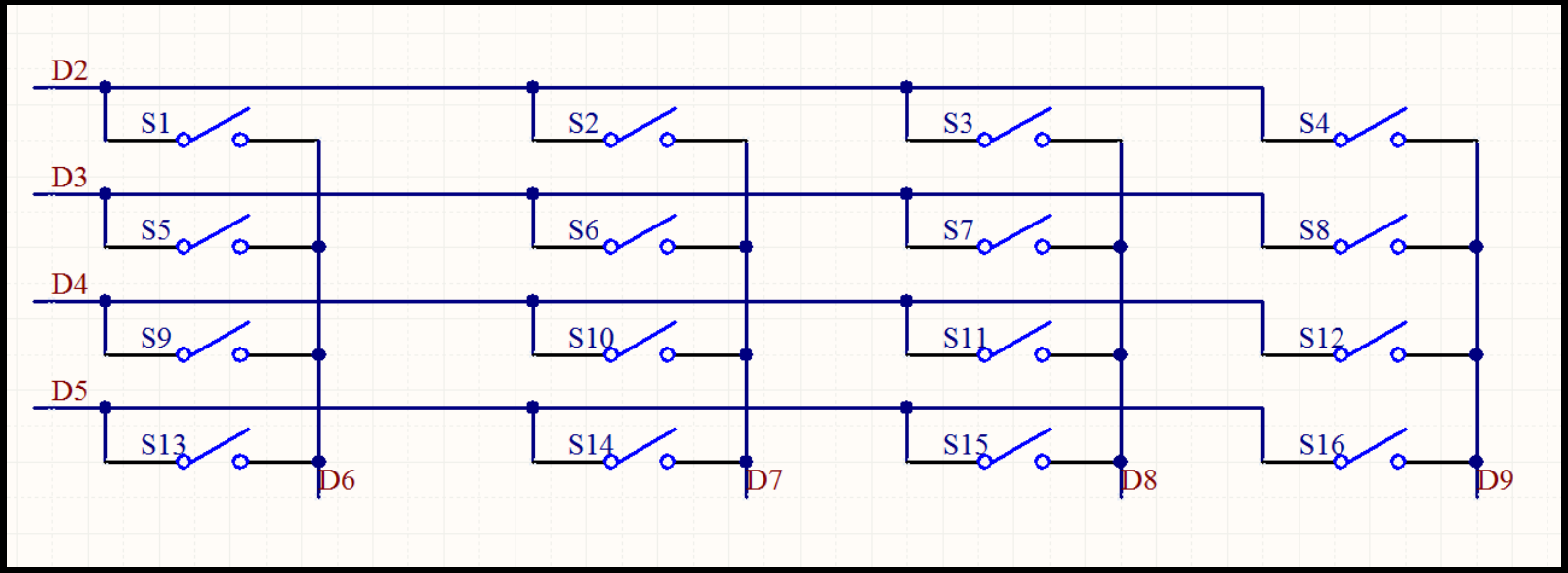
矩阵键盘原理



TEP #3

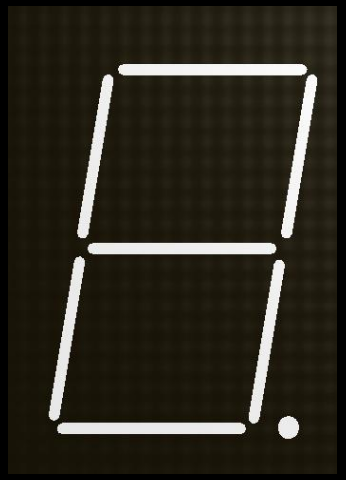

AN-L
AN_R
130123A_Y17
PotentialMeter
RP
S5 (7)
S9 (8)
S13 (9)
S6 (4)
S10 (5)
S14 (6)
S7 (1)
S11 (2)
S15 (3)
S8 (0)
S12 (.)
S16 (=)
S1
S2
S4
(+)
(*)
(/)
(-)

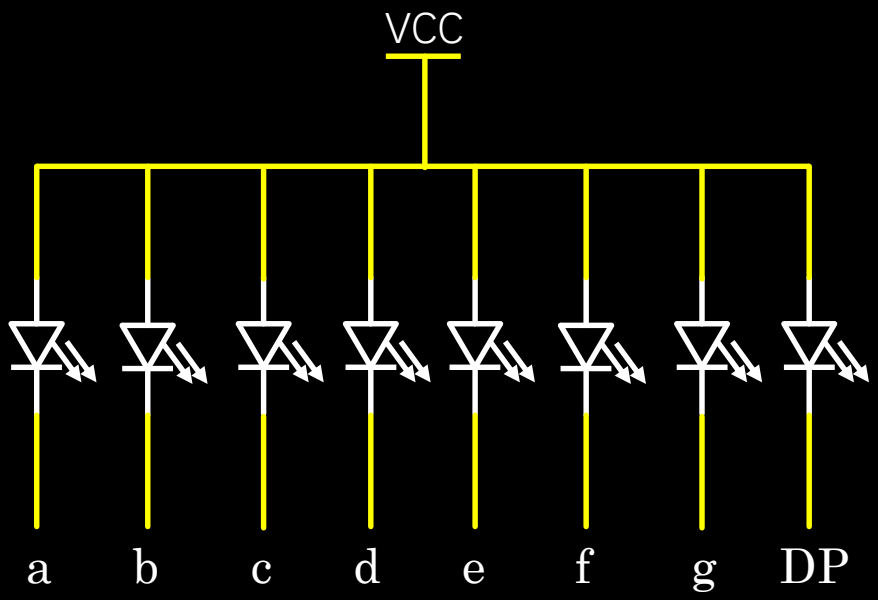
TEP #3 上面的矩阵键盘



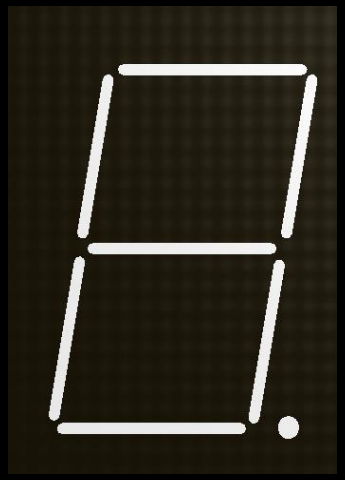
多位数码管怎么处理

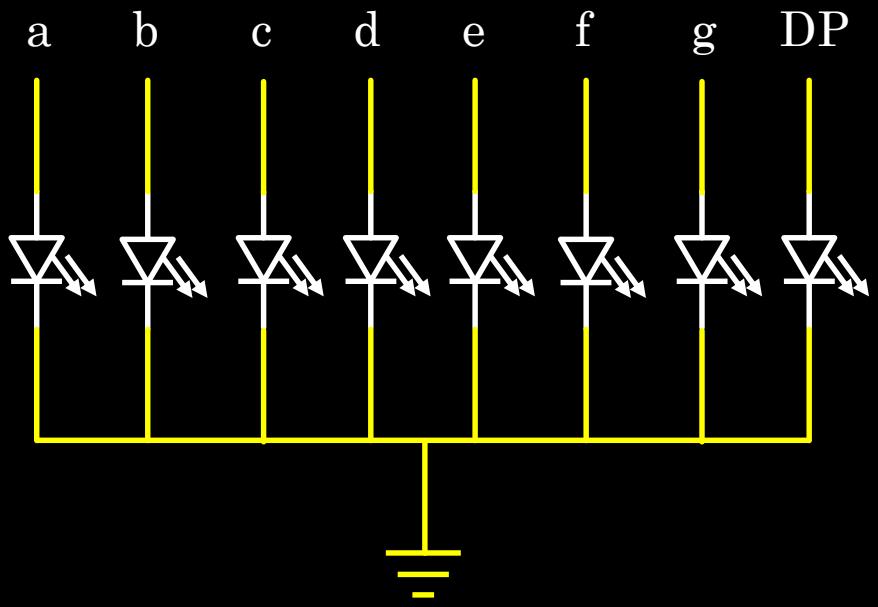
数码管

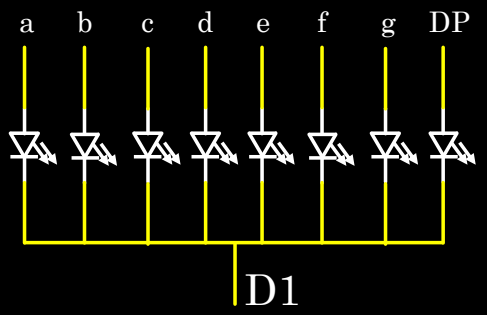


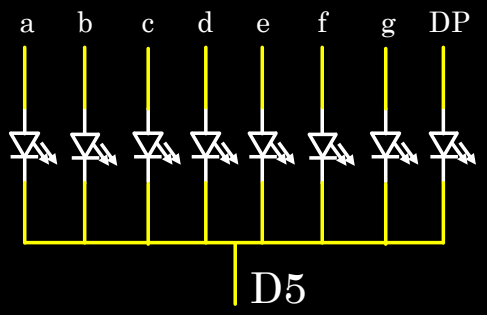


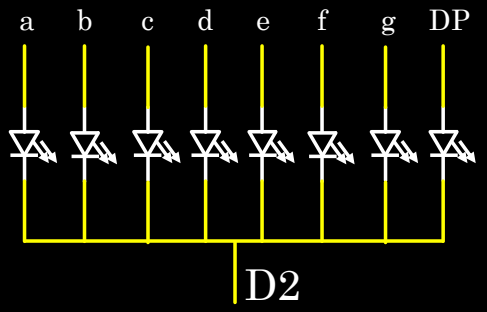
数码管

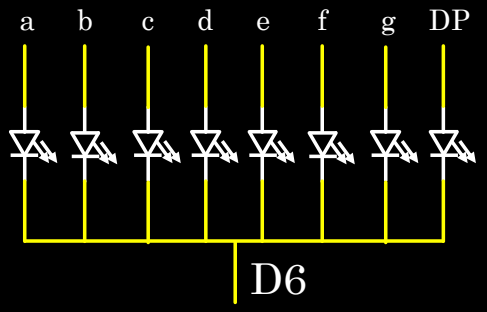


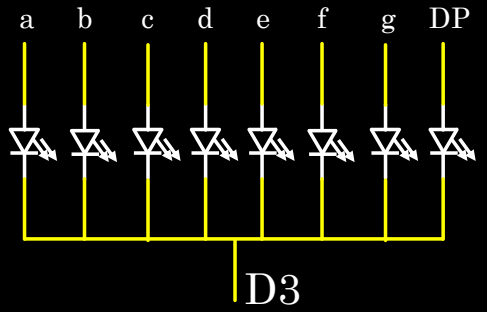


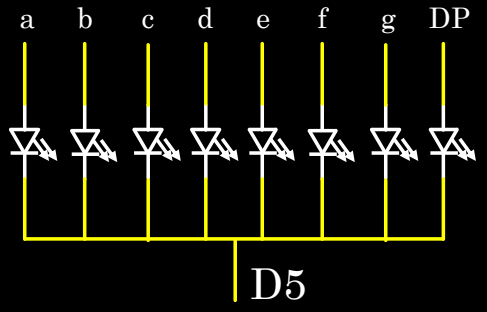

a b c d e f g DP
D1

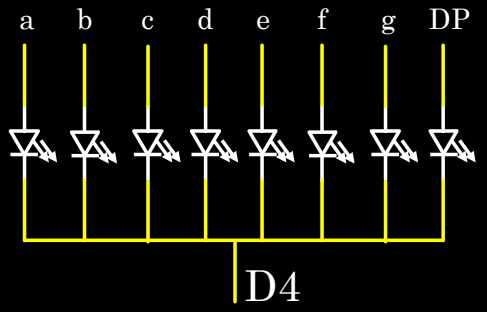

a b c d e f g DP
D5

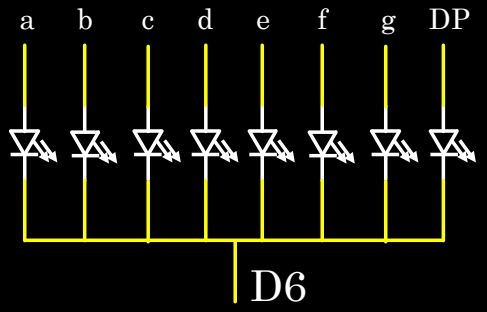

a b c d e f g DP
D2


a b c d e f g DP
D6


a b c d e f g DP
D3


a b c d e f g DP
D5


a b c d e f g DP
D4


a b c d e f g DP
D6

原理

- 通过视觉暂留现象欺骗人眼，达到多个灯同时亮的假象
- 怎么权衡扫描频率：
  - 理论上视频达到25fps以上就看不出特别闪烁了
  - 扫描频率不宜太快

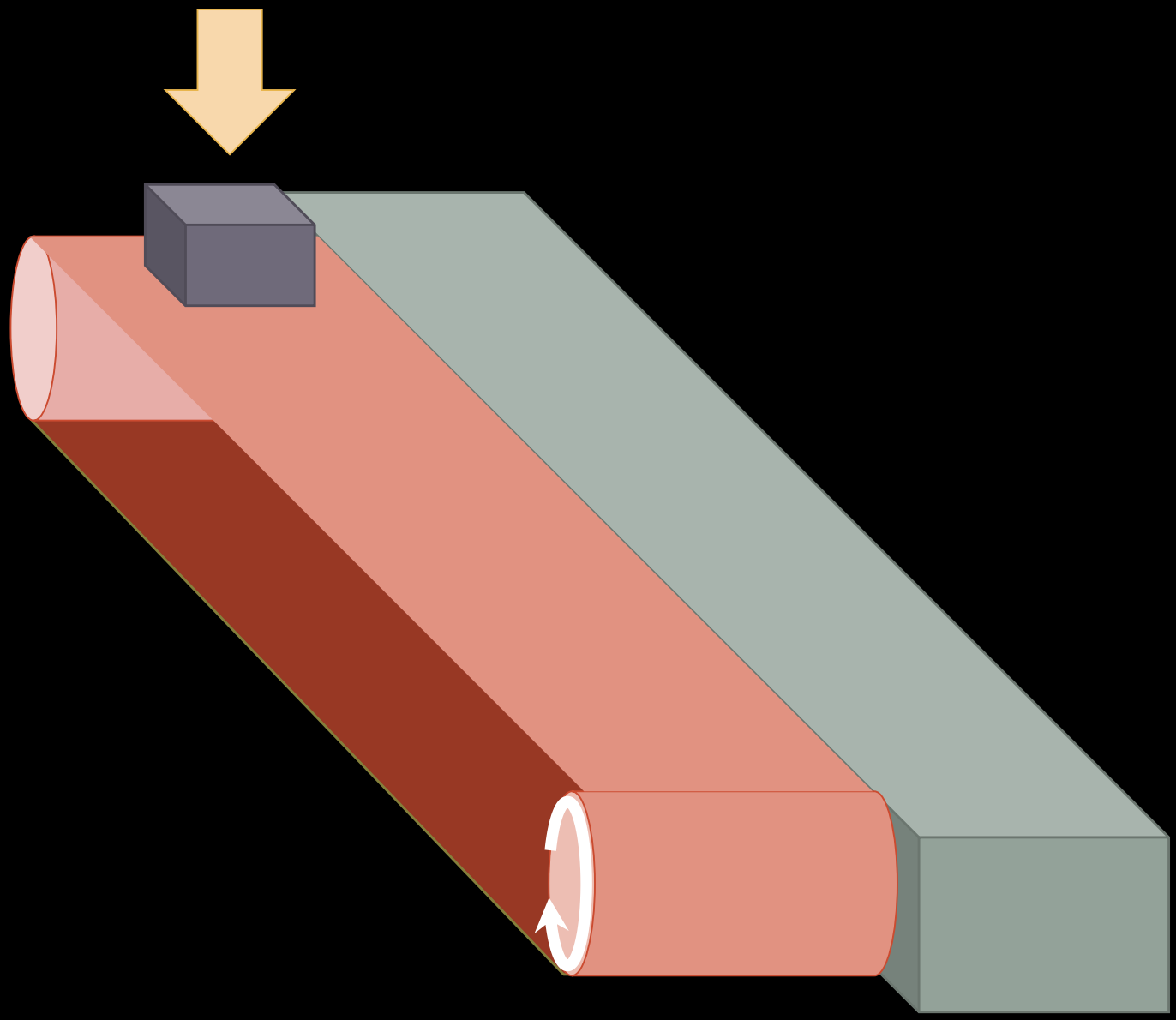
小结论

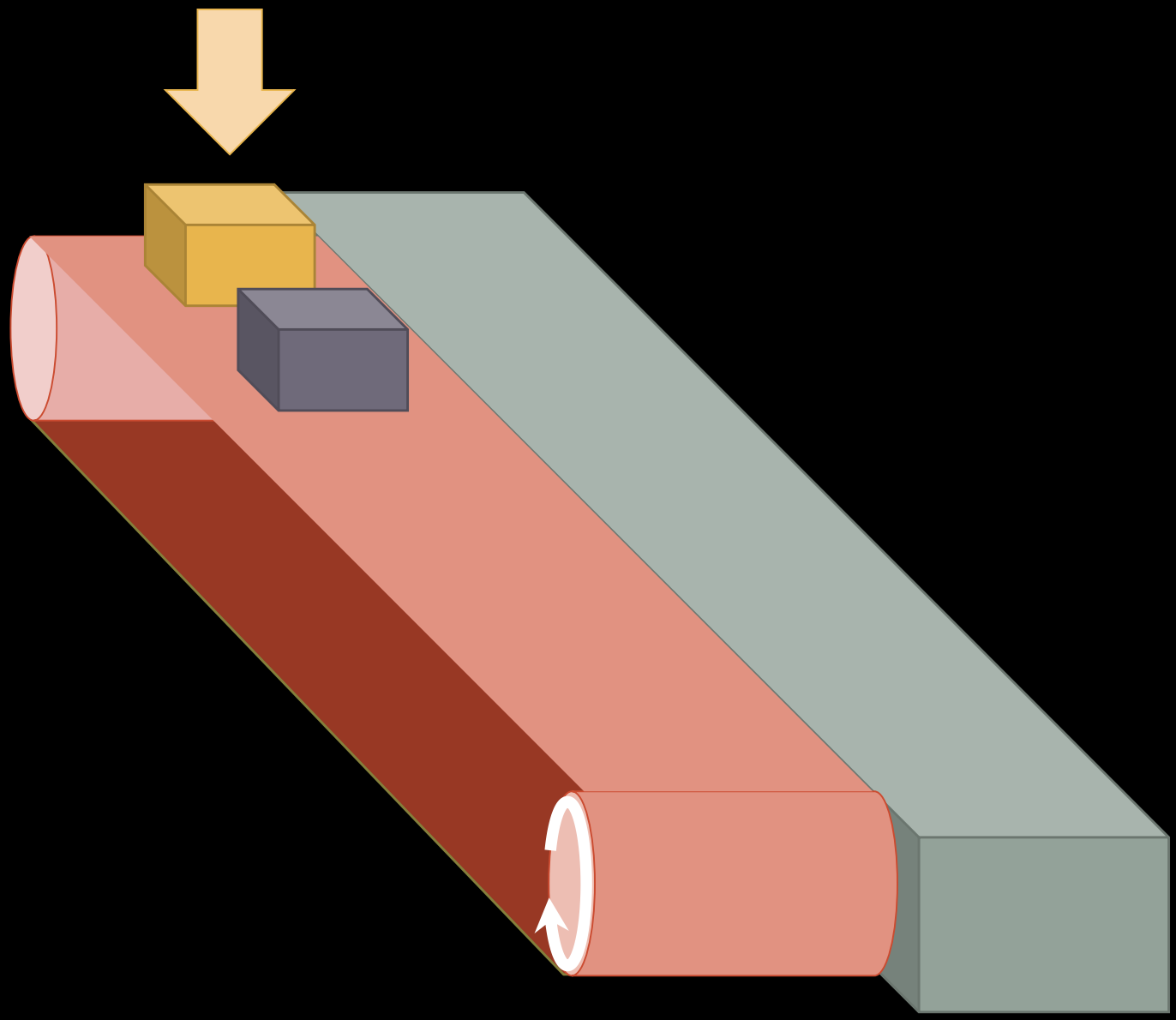
- 需要的引脚数
  - OUT　　数码管　　方法
  - 64　　8　　原始
  - 16　　8　　扫描
- 还能再少么？

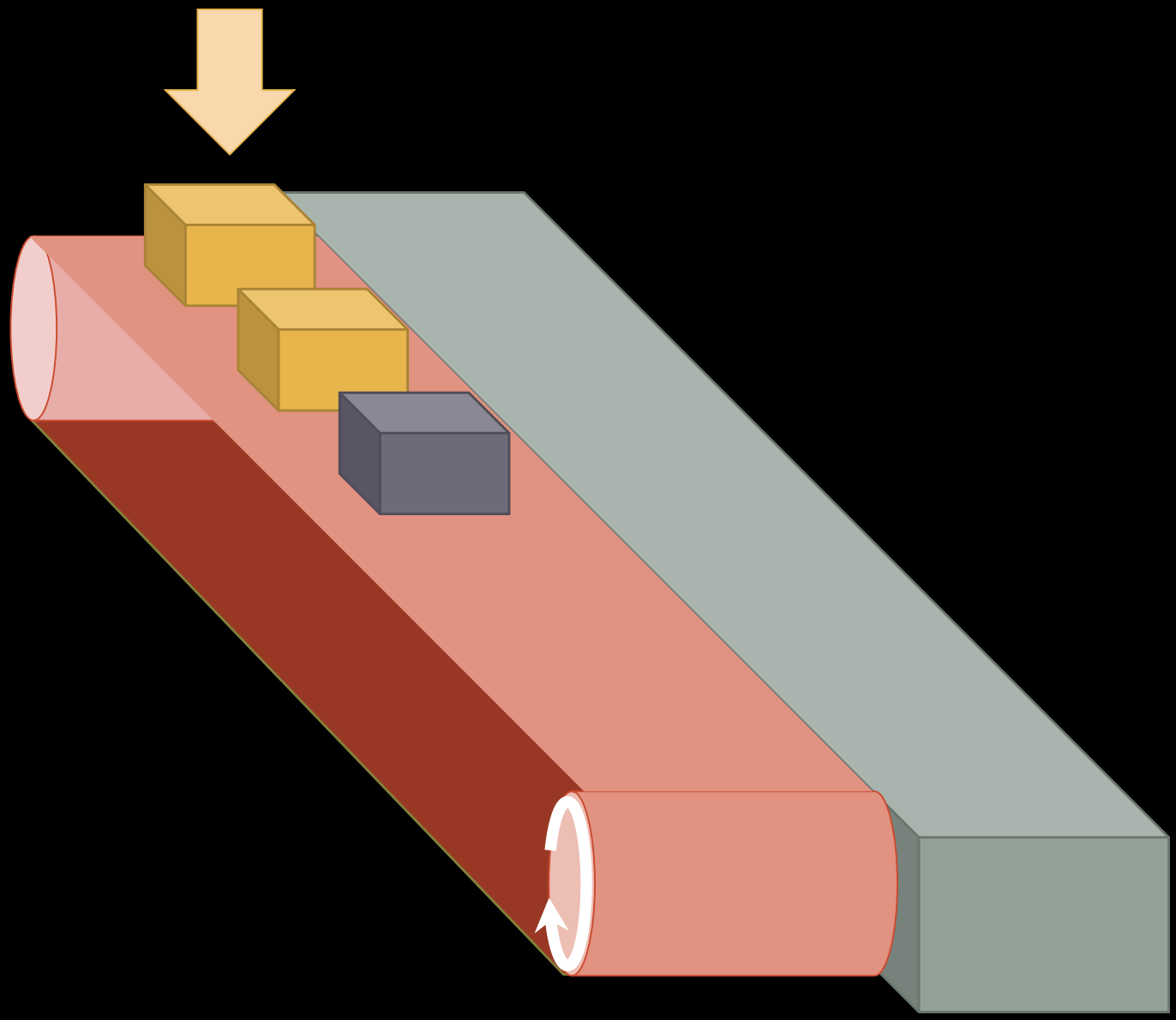
能

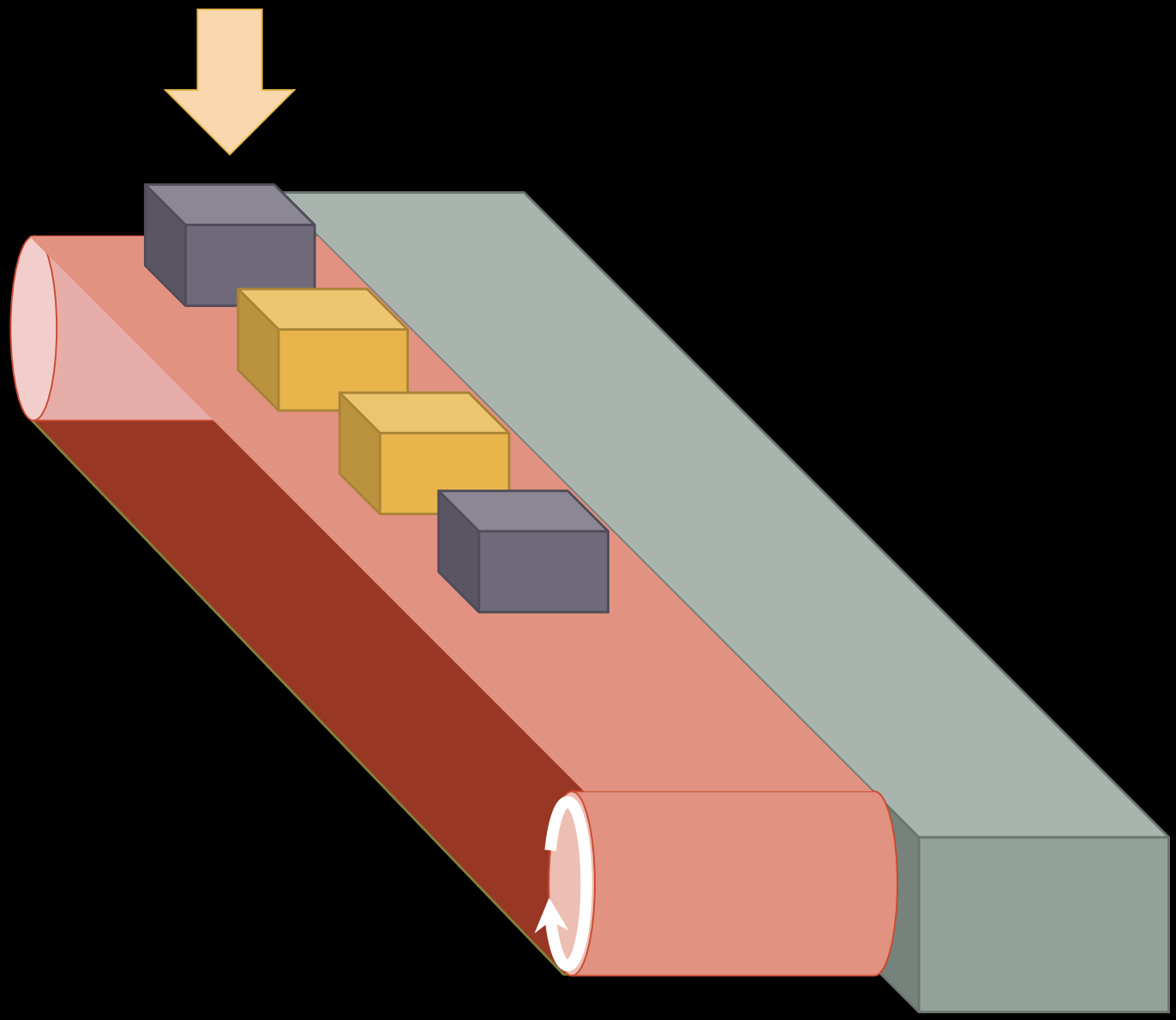
- 需要使用IC来实现
- 移位寄存器：串行和并行的互相转换

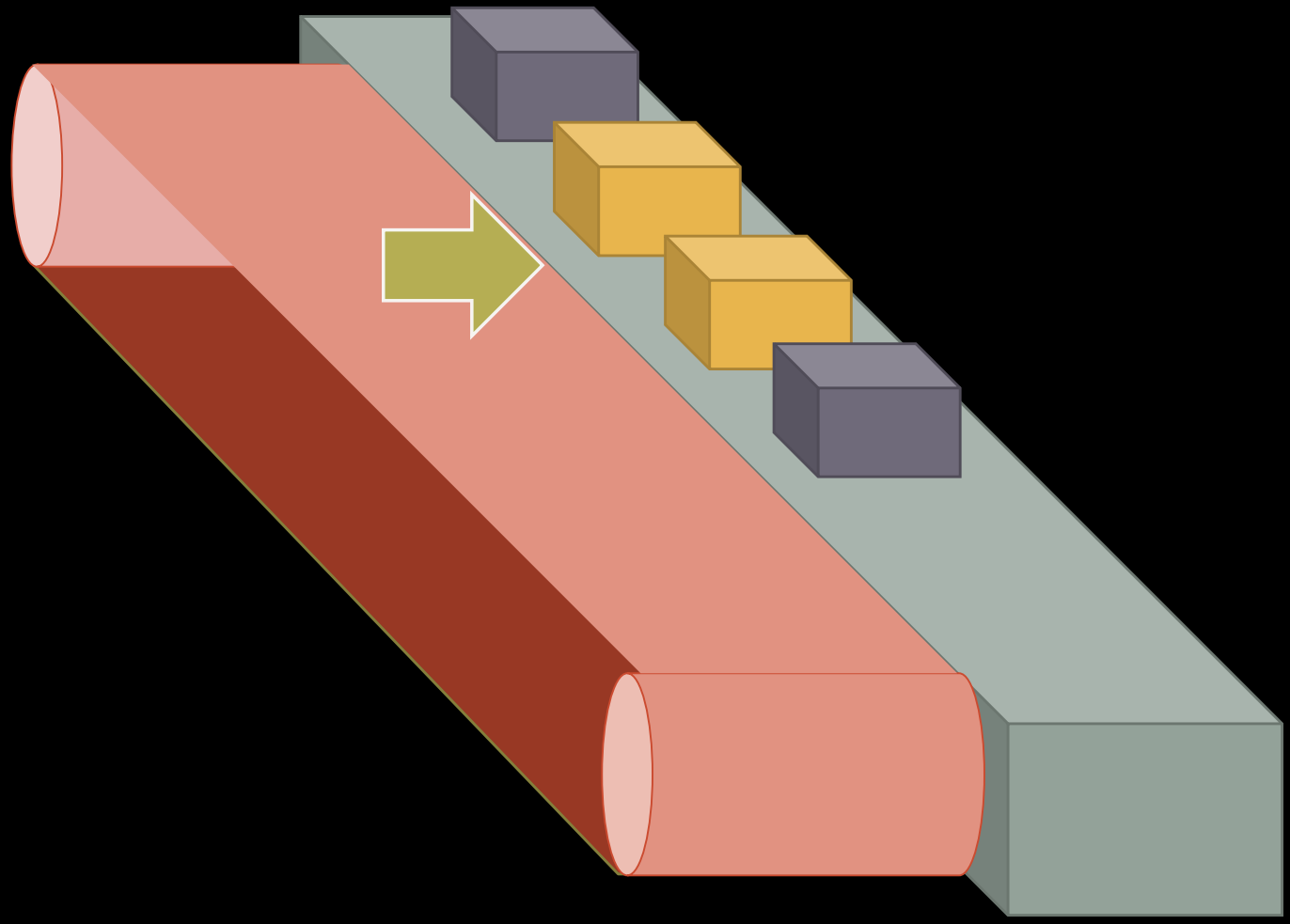
串进并出的移位寄存器



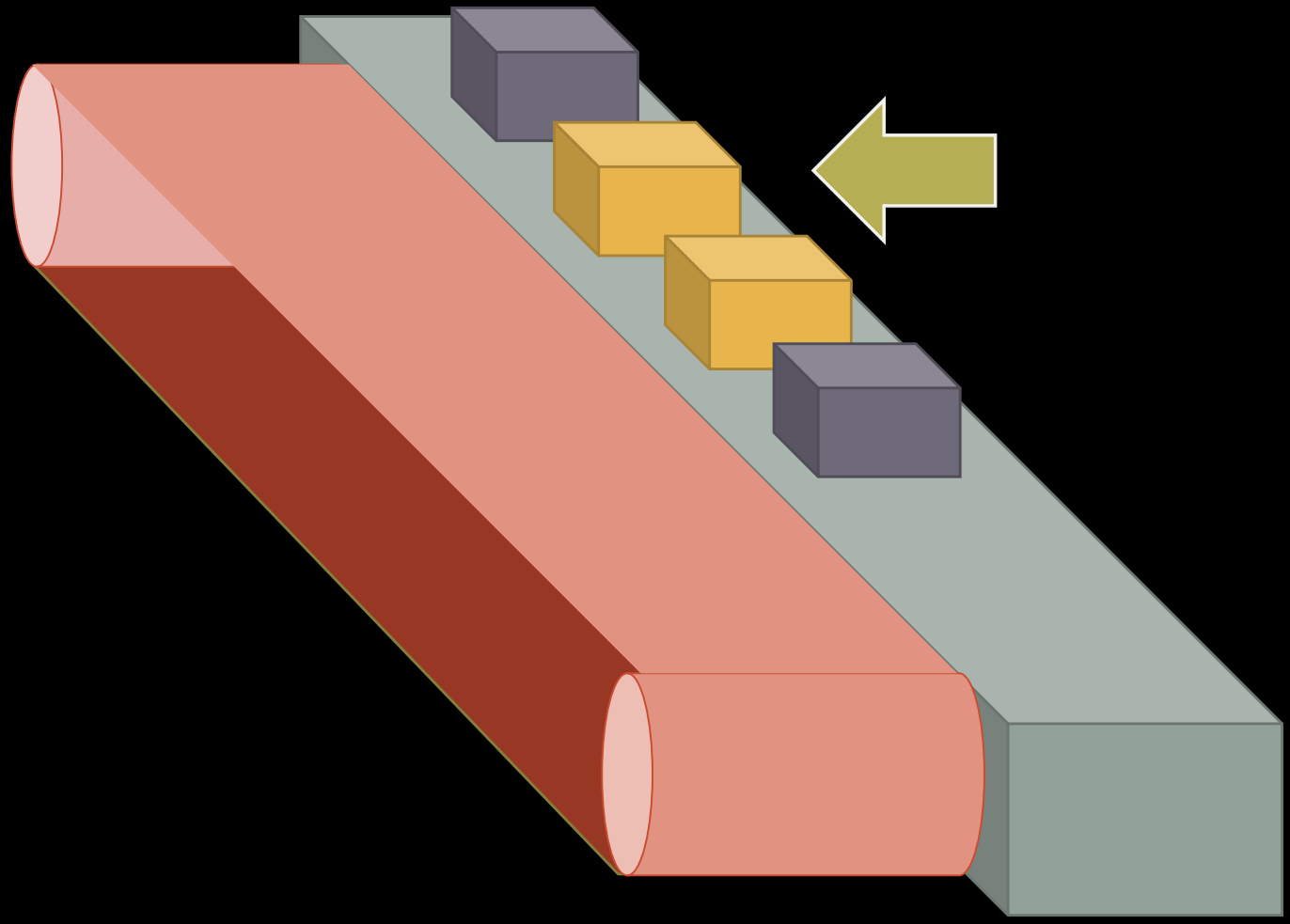


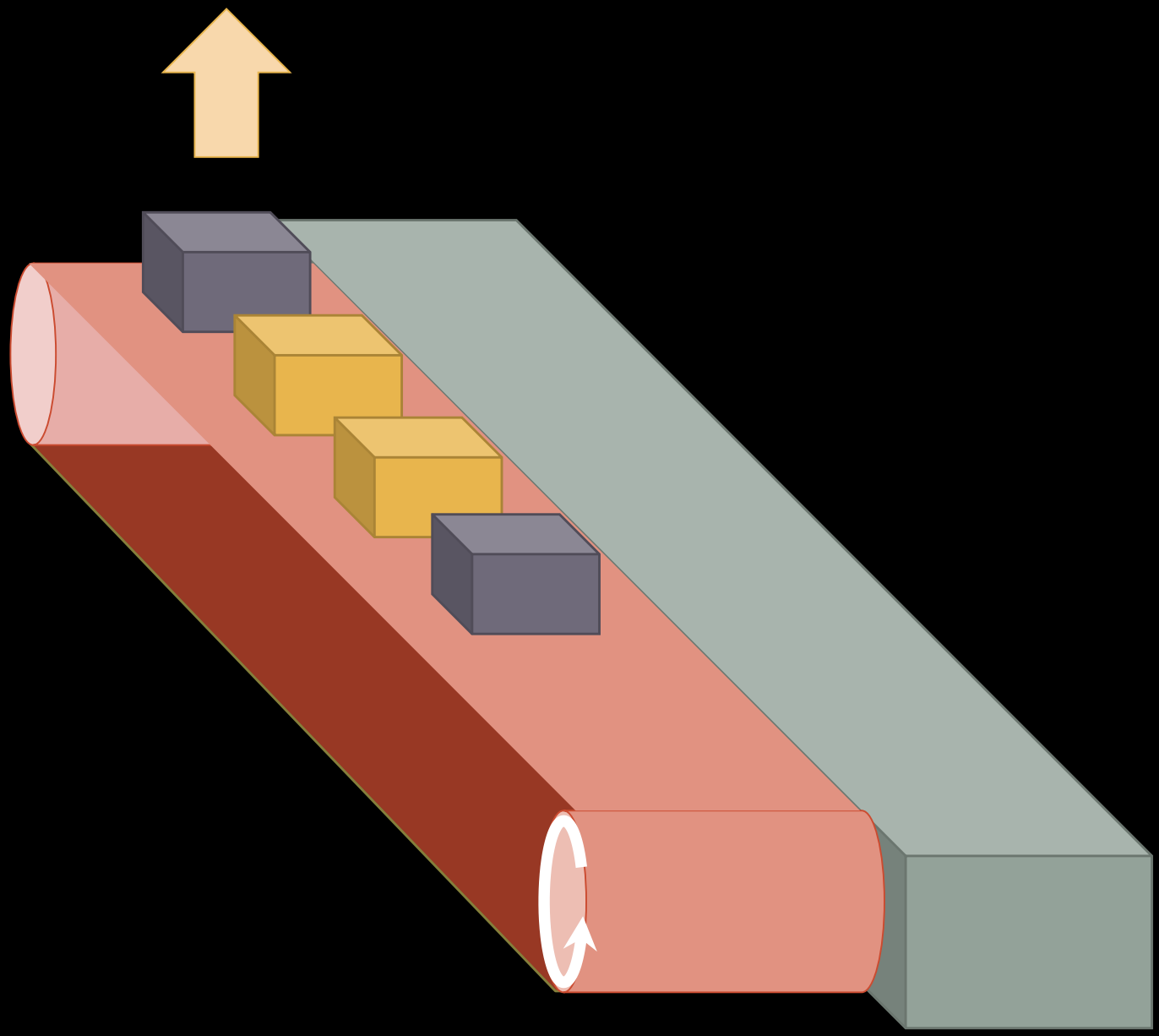


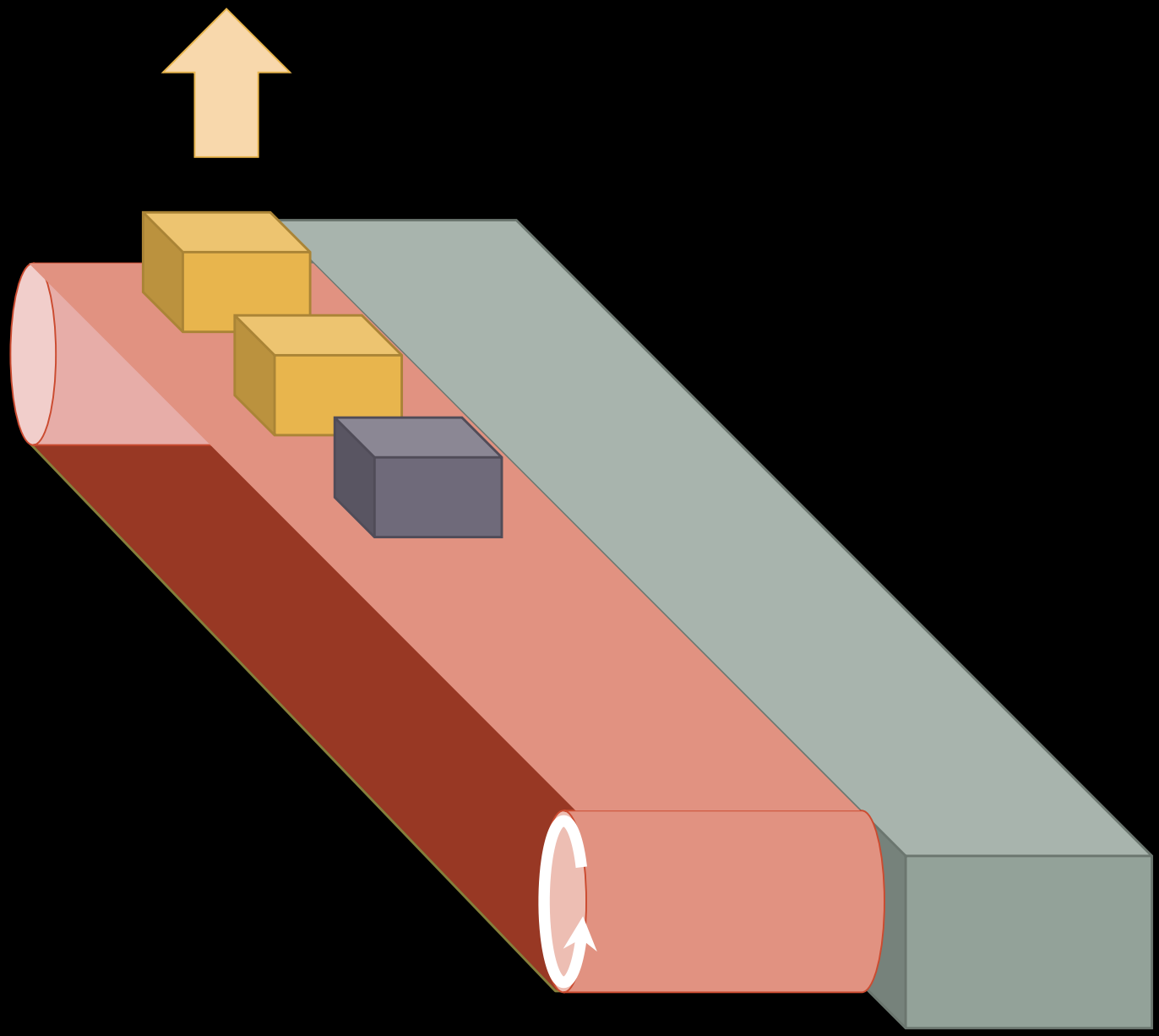


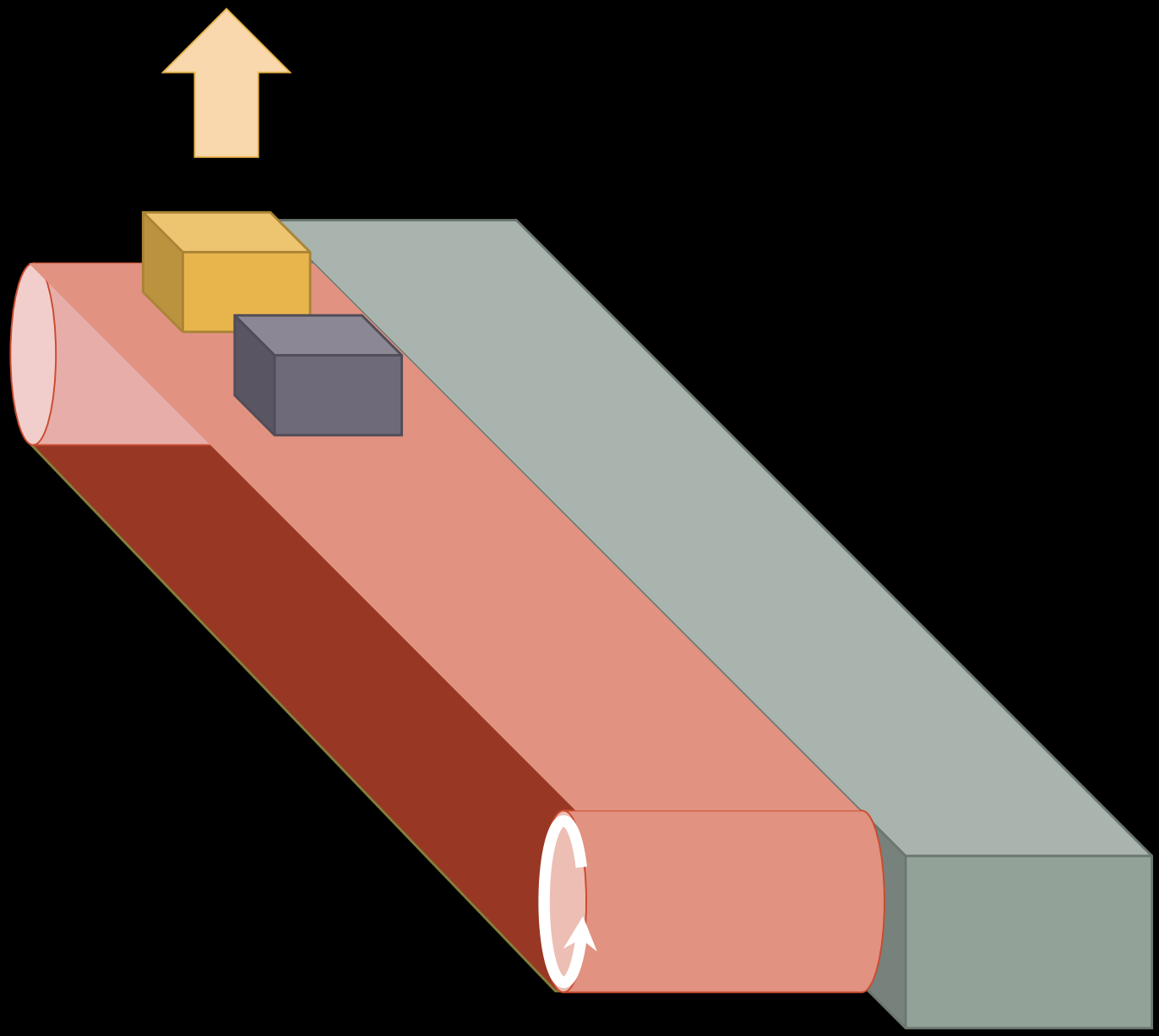


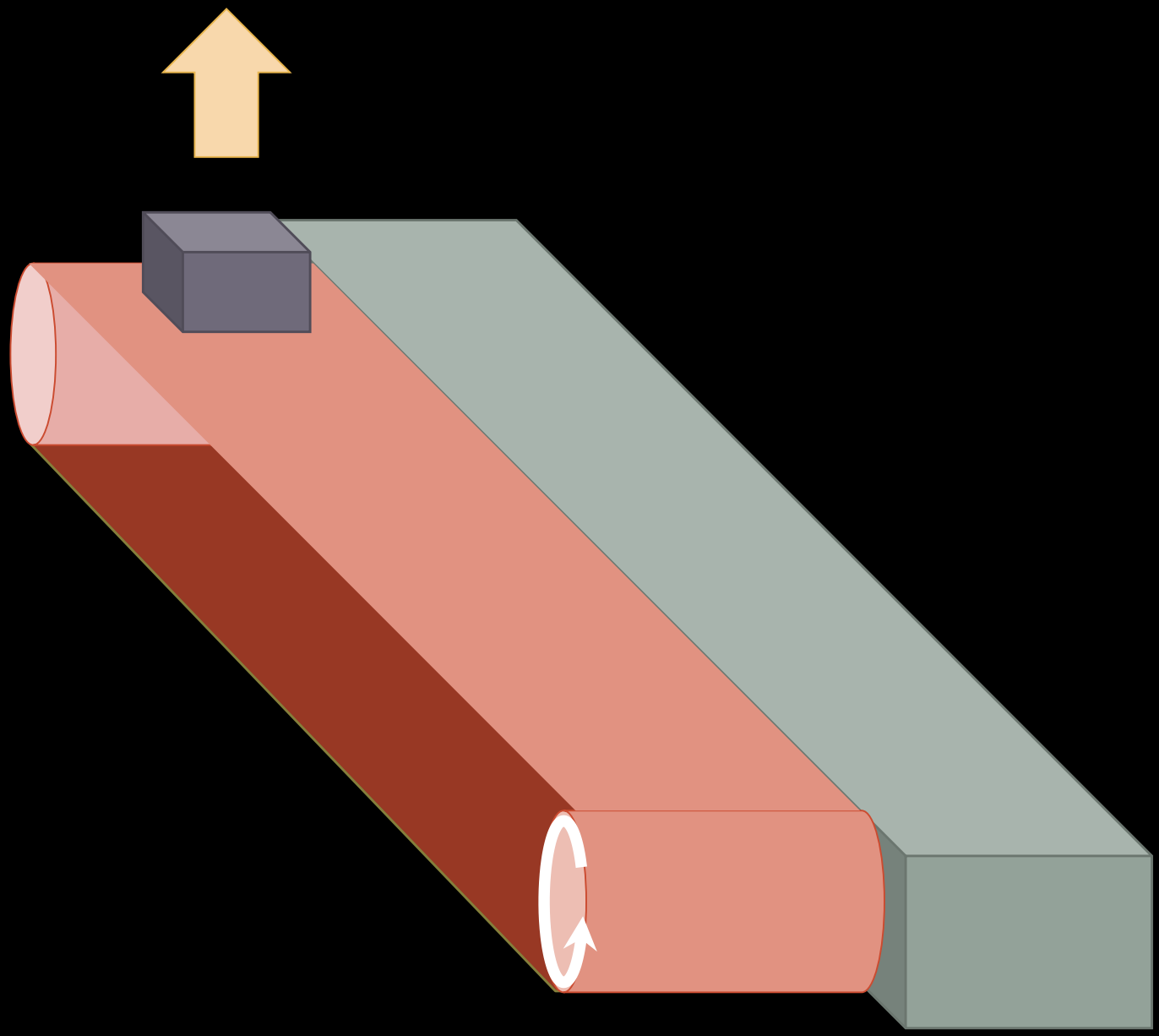
并进串出的移位寄存器





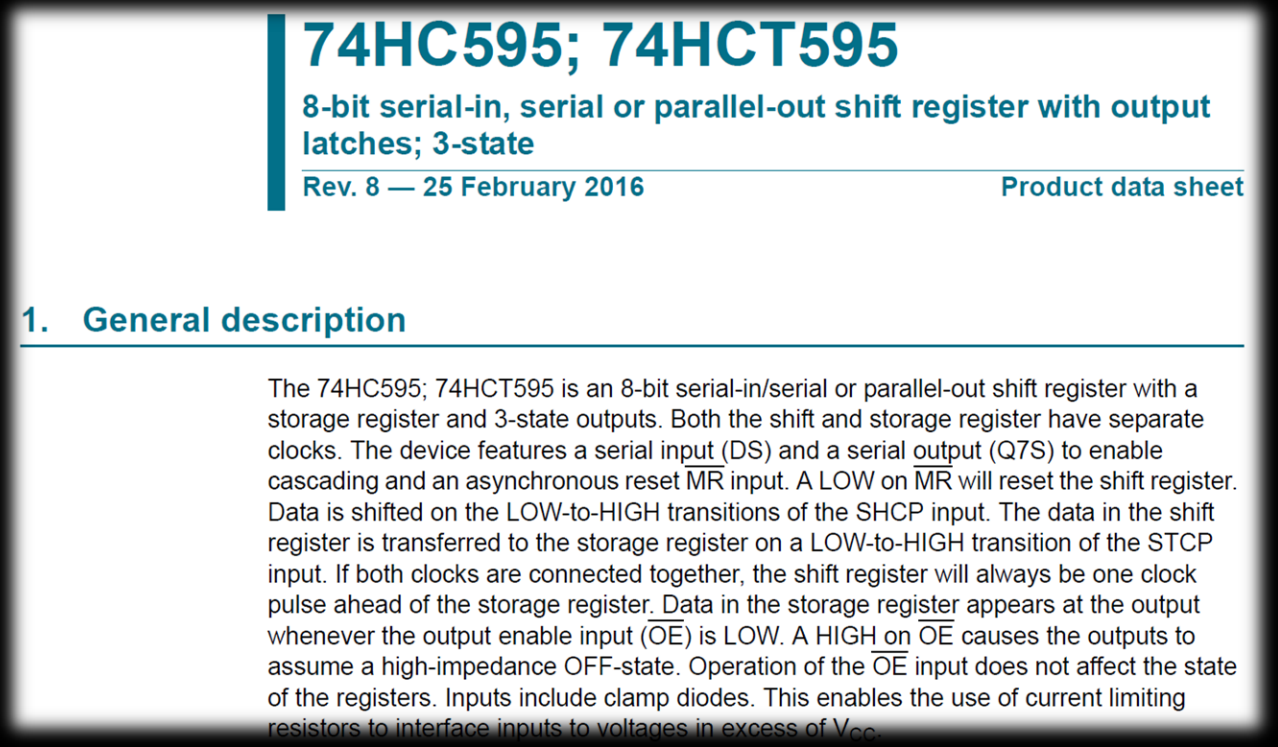






串进并出

- 代表芯片：74XX595



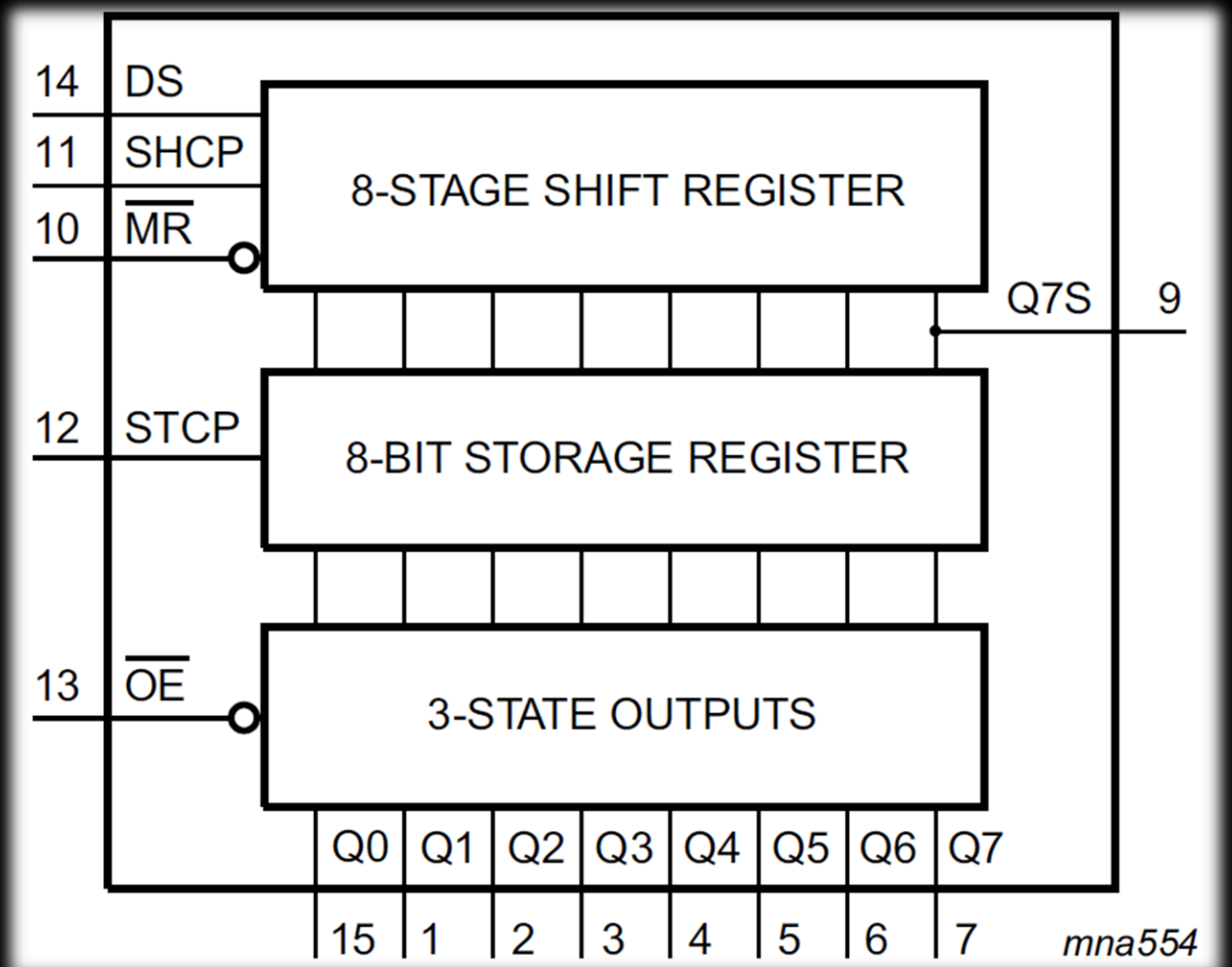
74HC595; 74HCT595

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

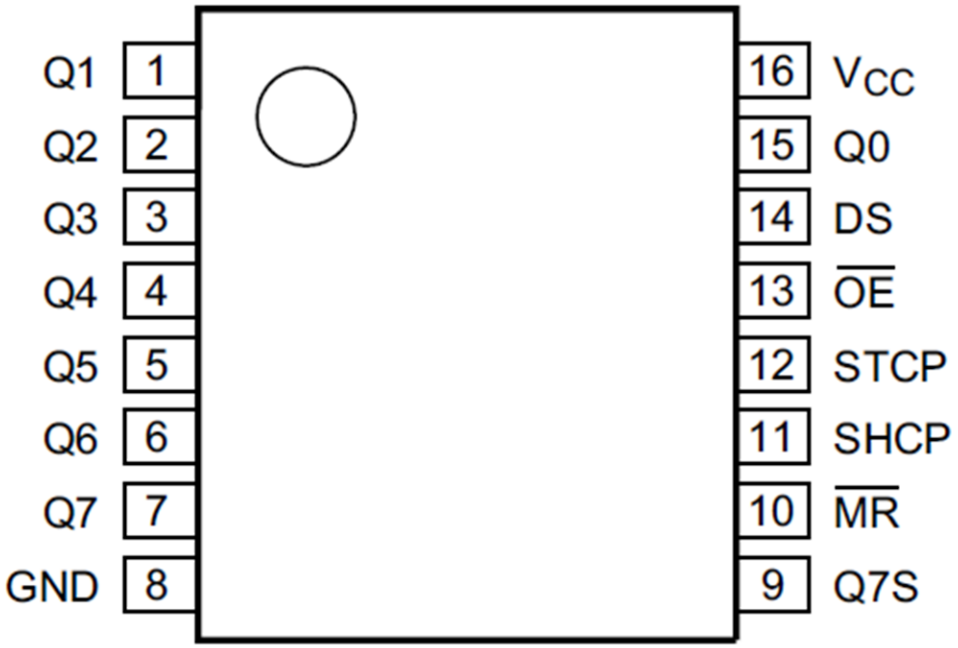
Rev. 8 — 25 February 2016 Product data sheet

1. General description

The 74HC595; 74HCT595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset $\overline{MR}$ input. A LOW on $\overline{MR}$ will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.


14
DS
11
SHCP
10
MR
8-STAGE SHIFT REGISTER
Q7S
9
12
STCP
8-BIT STORAGE REGISTER
13
OE
3-STATE OUTPUTS
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
15
1
2
3
4
5
6
7
mna554

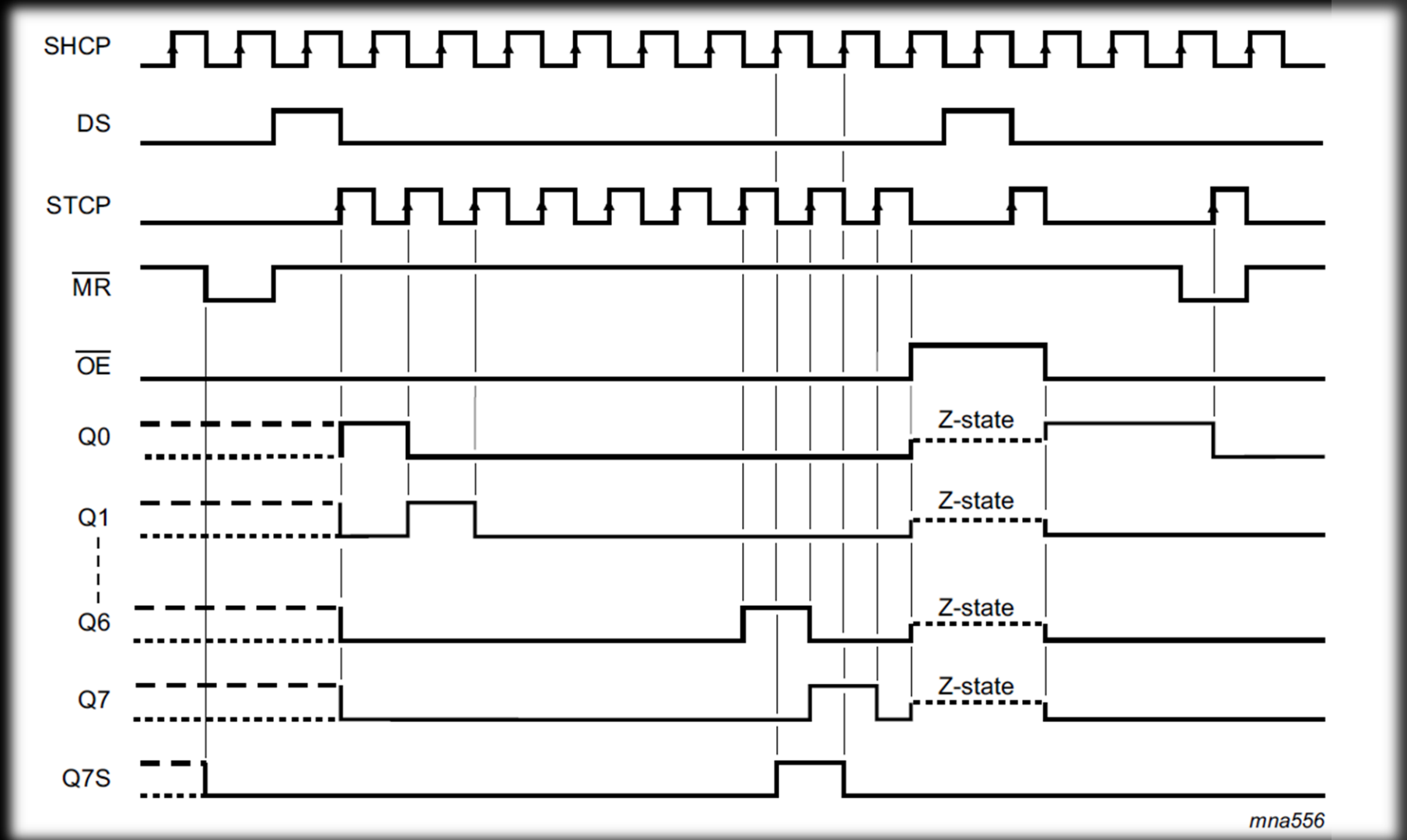
74HC595
74HCT595



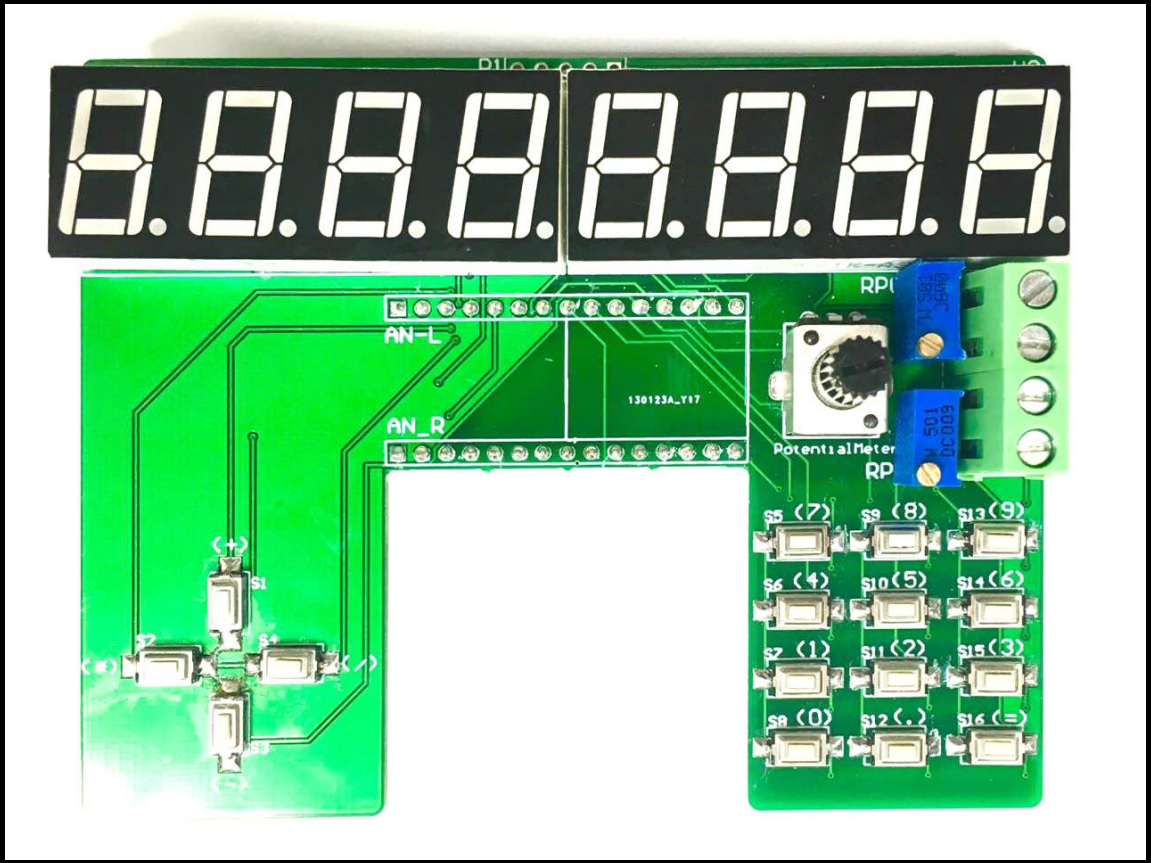
001aao242

Table 2. Pin description

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
$\overline{MR}$	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
$\overline{OE}$	13	output enable input (active LOW)
DS	14	serial data input
Q0	15	parallel data output 0
V_{CC}	16	supply voltage


SHCP
DS
STCP
MR
OE
Q0
Q1
Q6
Q7
Q7S
Z-state
Z-state
Z-state
Z-state
mna556

TEP #3 – 今日任务


AN-L
AN_R
130123A_Y17
PotentialMeter
RP
S5 (7)
S9 (8)
S13 (9)
S6 (4)
S10 (5)
S14 (6)
S7 (1)
S11 (2)
S15 (3)
S8 (0)
S12 (.)
S16 (=)
S1
S2
S4
(+)
(*)
(/)
(-)